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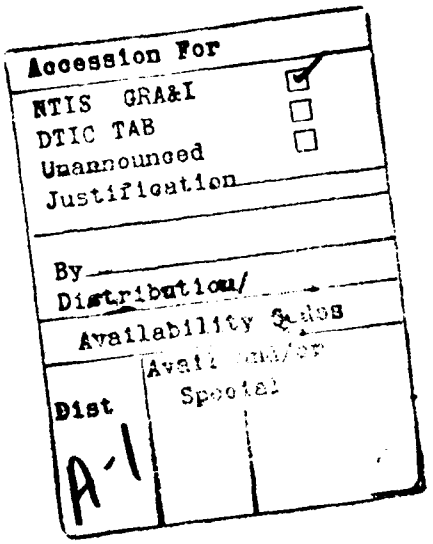

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INTRODUCTION

Adaptive receiving antenna arrays are electronic hardware and computer algorithms which are used to combine the radio frequency (RF) signals from several antennas in such a way as to provide an output signal with significantly enhanced signal-to-noise-and-interference ratio as compared to each of the individual signals from the separate antennas.

High-frequency (HF, covering the 2–30-MHz range in the U.S. Navy) adaptive receiving antenna array null steering can improve communications by increasing the signal-to-noise ratio. For shipboard adaptive arrays, this of course means suppressing intentional jammers (the primary objective for the array), but also includes suppressing on-board and off-board-generated interference and noise. Such arrays can also be used to separate multipath modes (for example, discriminating between surface wave and skywave propagation modes), since they are able to discriminate in elevation as well as in azimuth.

The HF adaptive antenna array (AAA) work within the Communications and Networking block program at NRaD is focused upon enabling technologies to support the shipboard introduction of an HF adaptive antenna array capability. To support the development and demonstration of these technologies, NRaD has implemented an adaptive array demonstration and evaluation test facility. This document describes the hardware and software implementation of a simulated array of four (or fewer) antennas. Simulated, rather than real, antennas are used primarily because they allow flexibility in implementing specific antenna configurations and individual antenna performance. In addition, simulated antennas are not contaminated by uncontrolled on-the-air noise and interference, thus allowing repeatability in the experiments.

A block diagram depicting the primary components of the adaptive array evaluation facility is shown in figure 1. The antenna simulator shown in the figure is an NRaD-fabricated device implemented specifically for the adaptive array evaluation facility. It simulates an arbitrary arrangement of one to four HF antennas. The user of the facility specifies the locations and characteristics of the antennas as part of an experiment definition computer file. The same file defines other characteristics of the experiment, including the directions of arrival (azimuth and elevation) of the various signals. The antenna simulator itself works on the assumption that the various signals are narrow band and that the antennas are in the far field of the various sources. Under these assumptions, the outputs from the various array antennas for a given source signal are just phase-shifted copies of one another. To generate these polyphase signals, the antenna simulator incorporates variable phase shifters that are remotely controlled by a Macintosh computer augmented with a suite of digital and analog circuit cards.

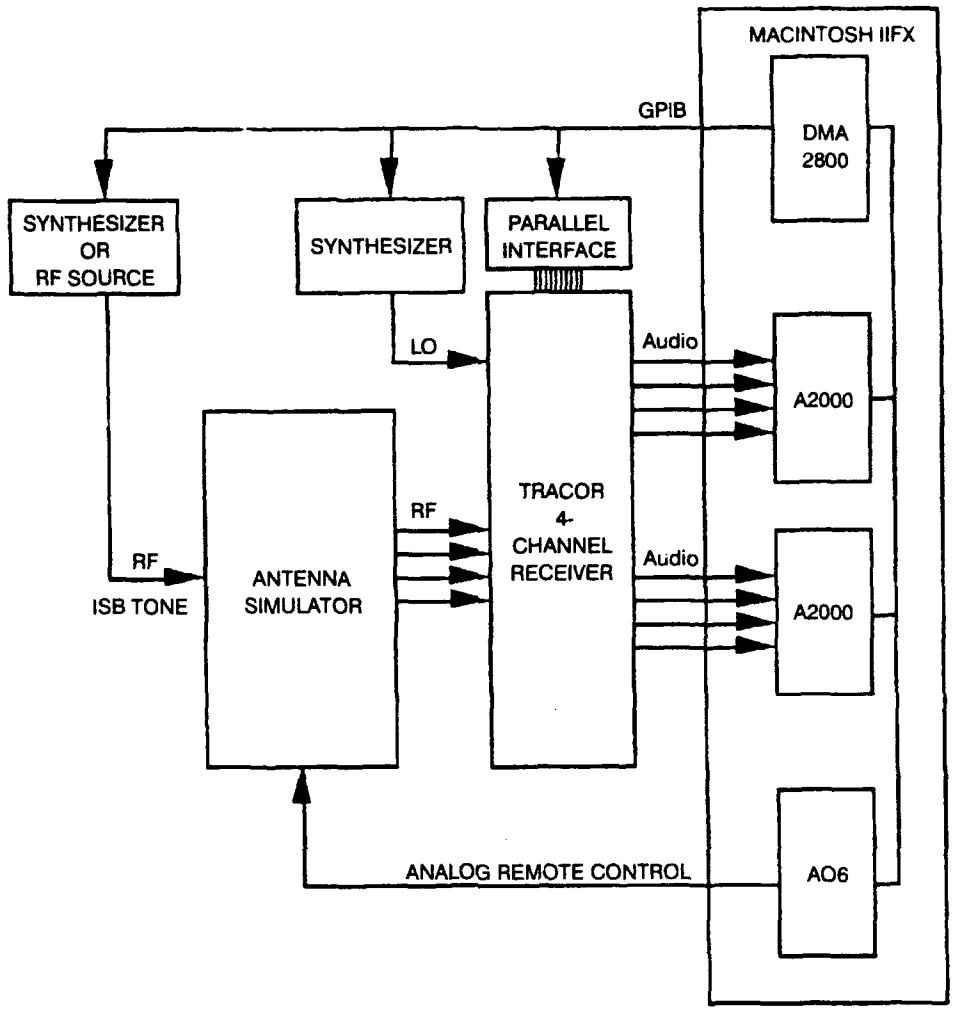

Figure 1. AAA evaluation facility, top level.

To simulate, say, a jamming signal output from the antenna array, software in the Macintosh computer calculates the phase shifts associated with each antenna, given the information on the antenna array geometrical configuration and the direction of arrival of the jamming signal. A test tone is applied to the antenna simulator at the required frequency, and the software then adjusts the various phase shifts in the simulator until the appropriate values are observed at the simulator output. This configuration is then maintained, and the input to the antenna simulator is changed to the signal for the current test (a jammer in our example). The antenna simulator outputs obtained as a result of these particular phase shift settings are used as RF inputs to the four-channel HF receiver during experiment data acquisition.

This document has been organized into five main parts. First, the design approach, which identifies the need for a special-purpose hardware device in order to generate the polyphase RF signals needed for antenna array simulation, is discussed. The design approach is followed by

two sections intended to provide broad-brush hardware and software overviews. In these two sections, the reader is introduced to the major hardware assemblies and software algorithms needed to implement the antenna array simulation, but the level of detail is kept to a minimum.

At this point, a detailed hardware description is introduced, complete with panel layouts, wiring diagrams, and schematics, which can be used as a guide for Simulator maintenance and troubleshooting tasks. A software section with similar detail follows and describes the phase-tuning algorithms used during experiment execution. Once the reader has completed these five main parts of the document, a brief conclusion and recommendation section is provided, followed by Appendix A. This appendix will be especially helpful to the reader who may be unfamiliar with LabVIEW, the graphical programming language software used to create the Simulator software algorithms. Appendix B is provided to include simulator circuitry schematics.

DESIGN APPROACH

To implement the Four-Channel HF Receiving Antenna Array Simulator, it is necessary to produce four independent RF signals with user-defined phase shifts between adjacent channels. For the generated RF signals to be an effective simulation, it is essential that the phase angle introduced on each antenna channel accurately depict the geometric scenario created by an approaching far-field wave front and the spatial orientation of the receiving antenna array. To this end, selectable experiment parameters, including incident signal direction of arrival and antenna array spatial location, are edited by the user at the beginning of each simulation session. A software algorithm resolves the antenna current phase angles for each emitter based on these user-defined parameters.

Once the desired phase angles are computed, each Simulator antenna output channel is tuned to replicate these exact RF output conditions. A narrow-band reference signal, centered in the receiver passband, is needed to initiate the phase-tuning process. This highly stable reference signal is generated by a remotely controlled frequency synthesizer using the General Purpose Instruction Bus (GPIB) and is provided as an RF input to the Simulator. The GPIB plays an important role during the tuning process by also controlling the receiver local oscillator synthesizer, the receiver attenuator, and the frequency-select parallel interface.

To generate the four-channel polyphase RF outputs, a special hardware unit is required. The special hardware unit passes the input RF reference signal through a four-channel RF power divider and subsequent phase-shift circuitry to generate the four antenna outputs with independent phase shifts on each channel. This special hardware unit is remotely controlled by an analog output port originating from within the Macintosh computer. The remotely controlled unit interactively converts the analog control voltages provided by the Macintosh computer into variable phase shifts on the four RF antenna output channels. To properly characterize the phase shift circuitry, a look-up table is created and stored on the Macintosh computer's hard disk. The table is tabulated in 5-degree increments throughout the entire 360-degree range. In this way,

the requested phase angles can be quickly set using an interpolation routine. Extensive software control system algorithms are incorporated to complete the four-channel RF phase adjustment process.

It is important to note, that each emitter present in the null steering/beam forming experiment is created individually using the Simulator, and the resultant data file is stored on the Macintosh computer's hard disk. Once the individual emitter files have been generated and stored, they are combined, sample by sample, to produce a composite file representing the total electromagnetic environment surrounding the simulated antenna array.

HARDWARE OVERVIEW

Of the many functional tasks performed during antenna array simulation, some lend themselves to hardware implementation, while others are more naturally completed in software. This is particularly true, since portions of the experiment simulation are completed in a controlled, non-real-time laboratory environment. Eliminating the real-time constraint allows a much greater portion of the workload to be performed by software algorithms, and minimizes the need for high-speed special-purpose hardware. A more detailed description of both the hardware and software attributes of the Four-Channel HF Receiving Antenna Array Simulator is provided in the following paragraphs, beginning with the hardware portion of the system development.

COMMERCIAL OFF-THE-SHELF HARDWARE

For those processes implemented in hardware, it was determined that all but one could be performed using commercial off-the-shelf (COTS) printed circuit boards. The processes implemented with COTS circuit boards include eight-channel data acquisition, analog I/O remote control, and GPIB (IEEE 488) instrumentation control. A suite of National Instruments printed circuit boards designed for use in Macintosh computer platforms met our project needs. For our implementation, data acquisition is performed by dual NB-A2000 four-channel data-acquisition boards. For analog remote control, an NB-AO6 analog output board is used. And for GPIB instrumentation control, an NB-DMA2800 GPIB controller board is used. All of these NuBus circuit boards are installed in the expansion circuit board slots inside a Macintosh IIfx computer.

The salient quality of these circuit boards is that each of them is supported by a software utility called LabDriver, which is the I/O controller portion of LabVIEW, the graphical programming environment used for simulation software development. The LabDriver utility is transparent to the LabVIEW software user and appears as a pallet of executable board support functions, which are capable of exploiting all the available hardware features a particular National Instruments board has to offer.

SPECIAL-PURPOSE HARDWARE

To implement the multichannel RF phase-shift capability, no off-the-shelf unit was available for our use. And although individual RF voltage-controlled phase-shift devices were available in the frequency range of interest, it was necessary to build a custom, multichannel, remotely controlled unit that could be configured by the operator using the graphical programming language software. The design and fabrication of this unit is described in greater detail in subsequent sections of this document. Together, this special-purpose hardware unit augmented by the suite of COTS circuit boards, a Macintosh computer, and the graphical programming language software, make up the Four-Channel HF Receiving Antenna Array Simulator.

SOFTWARE OVERVIEW

Although the processes implemented in hardware are discussed separately from the software routines, they should not be considered independent, stand-alone hardware modules. In fact, without the I/O driver and control system software routines, the hardware becomes virtually useless. It is only when the remotely controlled hardware, augmented by a suite of printed circuit boards, is driven by the graphical programming language software that the system becomes usable (see Appendix A). With this in mind, I will highlight the software routines that exercise the hardware circuitry and that make our implementation of antenna array simulation possible.

DATA ACQUISITION

The data-acquisition algorithm is fundamental to all other software processes used for the antenna array simulation. Acquired data is processed in many ways by several other Simulator routines. These routines include frequency and phase measurement, process control, and receiver audio output level measurement, to name a few. To initiate each of these processes, data are first acquired from the receiver baseband audio outputs across eight analog-to-digital input channels. These eight acquisition input channels correspond to the in-phase and quadrature audio outputs from the four-channel Tracor receiver, which is used exclusively for antenna array simulation.

To support the data-acquisition process, a portion of the Macintosh computer's random access memory is allocated as dedicated data-acquisition buffer space. This memory buffer space is logically oriented using a circular addressing scheme to allow for continuous uninterrupted data acquisition, once the process is initiated. As the buffer becomes filled to capacity with the most recently acquired data samples, the address pointer automatically returns to the first location in the buffer and begins to rewrite this previously used memory space. In this way, an epoch of the most recent receiver output events is stored and made available for block- or frame-oriented data extraction. This type of continuous background data acquisition followed by nonperiodic block- or frame-oriented extraction is particularly useful when a control system

process is implemented. The ability to quickly ascertain the effect of remote hardware adjustments using this type of data acquisition and extraction method was essential when the phase-tuning process incorporated in the antenna array simulation was implemented.

FREQUENCY ESTIMATION

Before phase measurements can be initiated, the frequency of the receiver baseband audio tone must be accurately known. The average frequency-estimator algorithm performs this task by acquiring samples of the receiver baseband audio output and applying signal-processing techniques to arrive at the estimated frequency. Built-in software functions are used to implement the signal-processing techniques.

To complete the frequency-estimation process, the array of sample data is windowed, passed through a Fourier transform, converted from rectangular to polar form, and stored in a one-dimensional array. The sample number of the array element with the maximum polar amplitude is multiplied by the acquisition sampling rate and divided by the overall number of array elements to arrive at the estimated frequency in hertz. This entire process is repeated (the number of times specified by the user) and averaged to obtain the average estimated frequency. Once an accurate estimate of the frequency is obtained, it is possible to estimate the relative phase shift between adjacent receiver channels. The average frequency-estimate algorithm is used by the phase-measurement algorithm during antenna array simulation.

PHASE ESTIMATION

The relative phase shift between adjacent receiver audio output channels is measured by the phase-estimation algorithm. To initiate a phase measurement on a given channel, it is necessary to first determine the frequency of the receiver baseband audio tone. Once the frequency of the signal is known, a quadrature pair of pure digitized sinusoids is generated at this frequency. The pure sinusoids are used as baseline reference signals, from which the relative phase shift of each receiver output channel will be measured.

In order to compute the relative phase shift between adjacent channels, the phase-estimation algorithm generates a series of trigonometric coefficients based on the two digitized sinusoids, and applies signal processing techniques to extract the phase information from the four-channel receiver baseband audio outputs.

GPIB REMOTE CONTROL

Several simulation processes are supported by remote instrumentation control using the GPIB. These processes include receiver local oscillator and RF signal generator control, as well as receiver-attenuator parallel-interface control. Each instrument connected to the GPIB has a

unique address, which allows broadcast bus commands to be received by the desired target device. Controlling remote instruments using the GPIB promotes ease of Simulator operation and assures experiment repeatability.

HARDWARE DESCRIPTION

The Four-Channel HF Receiving Antenna Array Simulator is a rack-mounted, remotely controlled unit that provides four RF outputs with user-defined phase shifts between adjacent channels. The unit is remotely controlled by a National Instruments NB-AO6 analog I/O circuit board operating inside a Macintosh IIfx microcomputer. The unit requires three electrical inputs: 120-VAC primary power, NB-AO6 analog control voltage, and the input RF signal of interest from which the phase-shifted versions are derived. A front panel houses the illuminated AC power switch and six red light-emitting diodes (LEDs) for display. Figure 2 depicts the Simulator front and rear panel layouts.

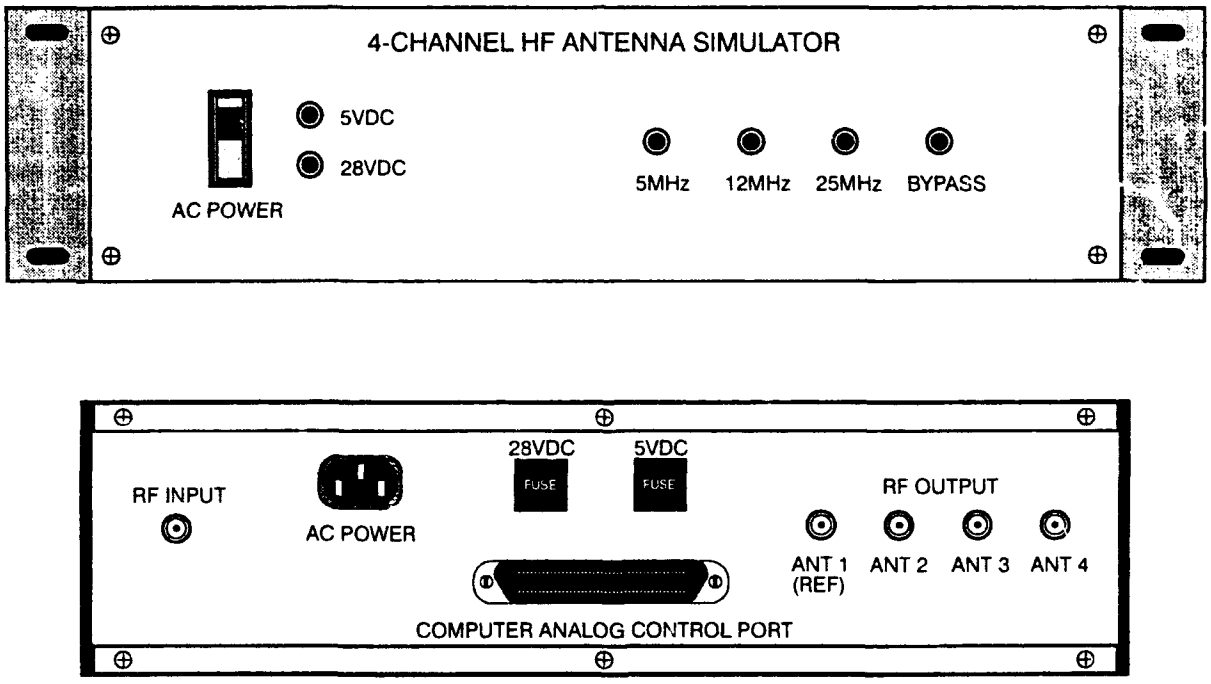

Figure 2. Simulator front and rear panel layout.

One feature of the Antenna Array Simulator is the ability it gives the user to control the unit remotely using National Instruments LabVIEW graphical programming language software. The flexibility provided by this software environment allows the user to easily change the phase-shift settings between adjacent Simulator channels by executing the appropriate virtual instrument (vi) on the Macintosh computer. The graphical programming environment encourages user-friendly interaction during program execution via the Macintosh display, keyboard, and mouse

When the vi software is executed, the NB-AO6 circuit board operating inside the Macintosh computer generates DC voltage levels at its output corresponding to values obtained from a phase-shift characterization look-up table. The table contains a complete listing of phase-shift drive voltages in 5-degree increments throughout the entire 360-degree range. For phase angles found between these 5-degree entry points, a linear interpolation is performed between adjacent table entries. The piecewise linear slope of the characterization curve in the area of the desired phase angle is maintained by the vi during execution, and is used to make phase corrections during the tuning process. Figure 3 shows a typical characterization curve segment with associated piecewise linear slope calculated in volts per degree.

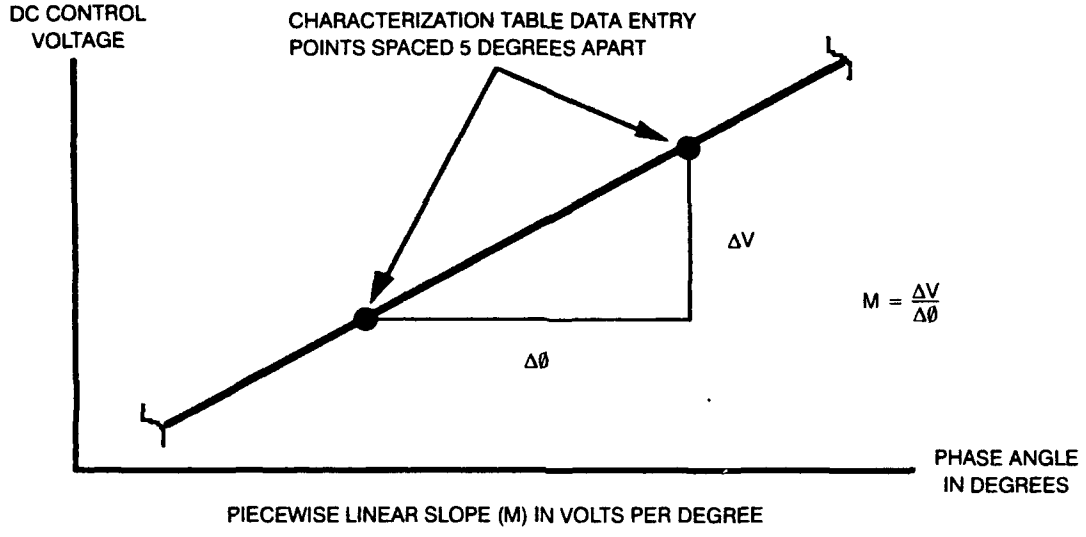

Figure 3. Phase shifter characterization curve segment.

Once the initial NB-AO6 voltage levels are computed and applied to the phase-shift circuitry inside the Simulator, the baseband outputs of the Four-Channel HF receiver are sampled using two NB-A2000 four-channel data-acquisition boards operating inside the Macintosh microcomputer. The measured phase angles on each channel are compared to the requested phase angles to determine the magnitude of the individual phase errors. If a given channel has a phase error larger than the user-defined resolution, additional phase tuning is automatically initiated. Automatic phase tuning is done by an algorithm that multiplies the individual phase errors (in degrees) with the characterization table piecewise linear slopes (in volts per degree) to derive the next set of output voltage settings. This process is repeated until the desired phase angles are achieved at the receiver output, which normally requires no more than two vi loop iterations.

HARDWARE COMPONENTS

The Four-Channel HF Receiving Antenna Array Simulator consists of a 19-inch rack-mounted chassis with display, +5-VDC and +28-VDC power supplies, a copper-clad wire-wrap circuit board, RF analog and digital circuitry, relays, fuses, connectors, and an AC EMI filter with power cord.

The heart of the Simulator is the voltage variable (voltage controlled) phase-shifter device. This RF device is used to vary the phase angle of the input signal based on the magnitude of the DC voltage applied at its adjustment terminal. The relative phase shift between the input and output RF signals is tunable over a 360-degree range by applying a 0- to +28-VDC control voltage at the phase-shifter adjustment terminal. To emulate a four-channel antenna array that can be tuned to one of three discrete RF frequencies, the Simulator utilizes three banks of voltage variable phase shifters, for a total of nine in all. Each bank consists of three individual phase shifters (one for each phase-tunable antenna channel), which are designed by the manufacturer to operate at a specific frequency. To cover the HF band, phase shifters were selected that operate at 5 MHz, 12 MHz, and 25 MHz with a usable bandwidth of approximately 10%. Figure 4 depicts the physical location of the phase-shifter banks within the Simulator chassis.

The RF signal applied to the input of the Simulator is distributed to the phase shifters by a four-way, broadband, RF power divider and a relay switching network. One of the four power-divider outputs is routed directly to the Simulator antenna output without introducing a phase shift and is used as the zero-phase reference for the three remaining output channels. Three of the four power-divider outputs are routed, via a relay switching network, to the selected phase-shifter bank, thereby providing the phase-shifted versions of the original RF signal at the Simulator antenna output.

The DC control voltage required to drive the phase-shifter devices is provided by three +28-VDC level-shifting networks, which are located on the wire-wrap circuit board inside the Simulator chassis. The level-shifting networks amplify the 0- to +10-VDC NB-AO6 output to the 0- to +28-VDC level needed to drive the phase shifters throughout their entire range. A 14-VDC regulator circuit provides the necessary mid-point biasing for the level-shifting networks. The NB-AO6 circuit board within the Macintosh computer is connected to the Simulator chassis via a multiconductor cable and connector.

The Simulator front panel display provides visual status for both the +5-VDC and +28-VDC power supplies, as well as the selection of the operating center frequency or bypass condition (no phase shift introduced on any channel). Primary AC power status is provided by the illuminated front panel AC power switch, which is green when active. The front panel display LEDs are red when active.

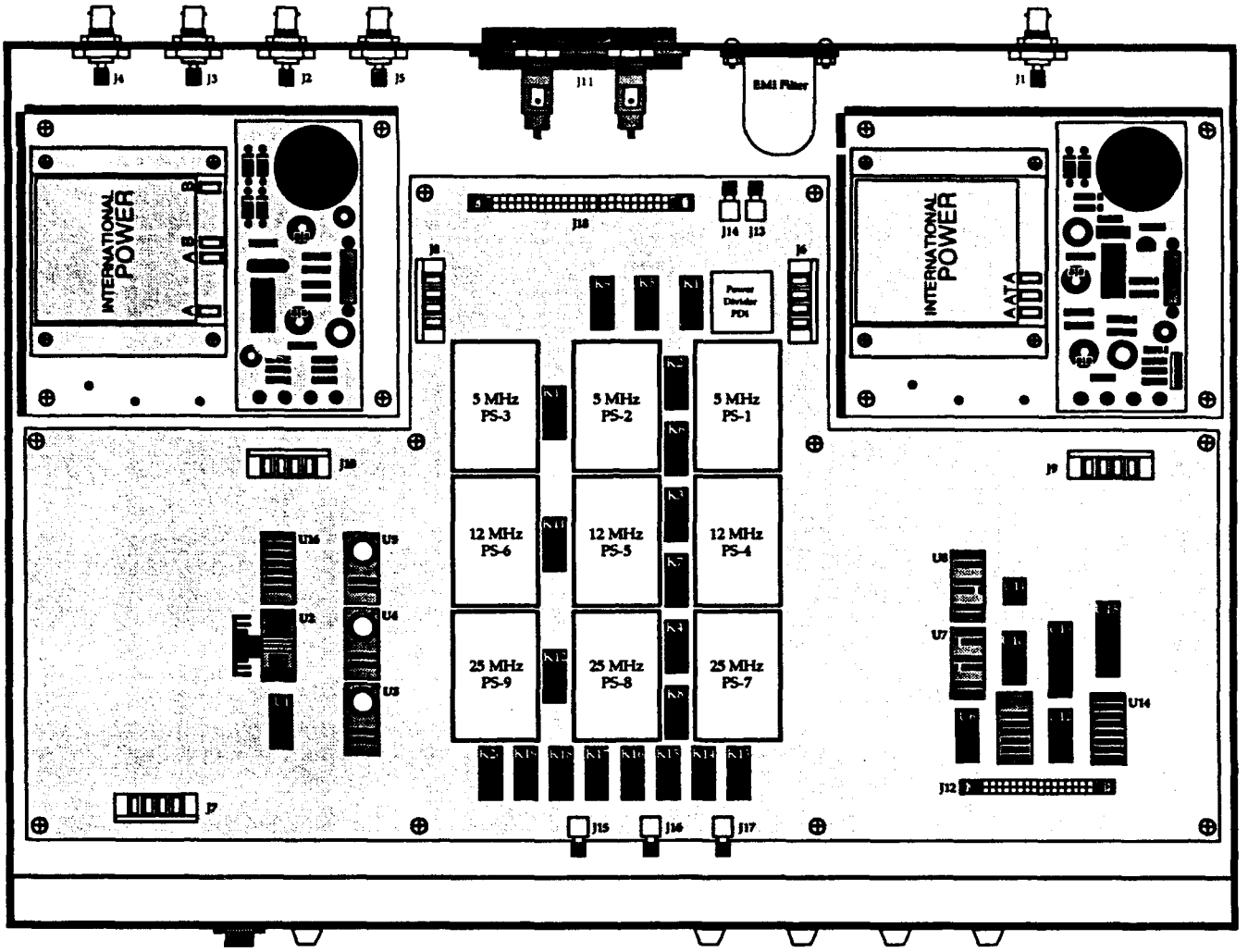

Figure 4. Simulator component layout.

Display control voltage levels are initiated by the NB-AO6 circuit board within the Macintosh microcomputer. Under software control, two of the NB-AO6 analog output channels produce transistor-transistor-logic (TTL) compatible voltage levels, creating a two-bit binary word. The decoded binary word is used by the Simulator to energize the appropriate phase-shifter bank-select relays and to drive the front panel LED display circuitry.

HARDWARE DESIGN AND FABRICATION

The Four-Channel HF Receiving Antenna Array Simulator was fabricated using a modular design. All major subassemblies within the unit are connectorized and can be removed without desoldering. A single copper-clad circuit board houses all RF, analog, and digital circuits within the Simulator. The integrated circuits and miniature analog networks are seated in dual-in-line (DIP) type wire-wrap sockets to facilitate removal and repair. The wire wrap side of the copper-

clad circuit board is clearly marked with designating pin numbers for identification. Interconnecting cables for RF, digital, and analog signals can be disconnected and removed without desoldering, which aids in testing, troubleshooting, and RF signal injection.

The copper-clad circuit board is perforated with tenth-of-an-inch hole centers, and has been machined to remove the copper coating where nongrounded circuit connections pass through the board. The remaining conductive surface area of the board is bonded (wired) to the ground connection of the input AC line. This copper-clad ground plane provides a suitable low-impedance path to earth ground for the input RF connectors, RF power divider, and voltage-variable phase-shifter devices.

Wire-wrap circuit connections are made using 28 AWG (gauge) strip-and-wrap-type wire wound on 0.025-inch square posts. This wiring technique is used for all circuit board connections except the primary AC power and front panel display circuitry, which uses 18 AWG stranded wire that is soldered directly to the connector sockets.

DETAILED CIRCUIT DESCRIPTION

Relay Switching Networks

Relay-switching analog control signals originating from the NB-AO6 circuit board inside the Macintosh microcomputer enter the Simulator through rear panel connector J11, pins 28 and 36. A 40-pin, mass-terminated ribbon cable, W6, connects the rear panel jack to the internal wire-wrap circuit board at connector J18, while maintaining the original input connector wiring pinouts. Refer to figure 5 for the Simulator RF and analog interconnecting wiring diagram. The TTL-compatible analog signals are hard-limited by voltage-limiting circuit U7, which consists of two 10K current-limiting resistors, U7e and U7h, and two 1N750, +4.7-VDC zener diodes, U7d and U7g. Refer to figure B-1 for the relay and display control schematic diagram. The conditioned signals at the output of U7, pins 9 and 12, are shaped by two inverting Schmitt-trigger gates, U10.

Together, the two output signals at U10, pins 6 and 8, form a two-bit binary word that is provided as an input to the two-line to four-line decoder U13. The decoded output signals at U13, pins 4 through 7, are buffered by octal buffer line driver U15 and provided as inputs to biasing resistor network U14. The high-active TTL signals originating from U15 provide forward-bias current to the selected transistor pair within the NPN transistor array, U6 and U12. Biasing network U14 establishes the base-emitter voltage drop across the selected transistor pair, which in turn enables the correct bank of frequency-select relays and drives the appropriate front panel display LEDs. Resistor network U9 limits the LED forward-bias current to optimize light emission while extending the device life span. Figure B-2 shows the relay switching interconnecting wiring diagram.

RF Power Division and Phase Shift

RF input signals are injected at the RF Input connector J1. The RF input signal is routed from connector J1 to the wire-wrap circuit board via RF cable W1 to connector J13. Refer to figure 5 for the RF and analog interconnecting wiring diagram. From connector J13, the signal is hard-wired to the input terminal of the four-way power divider PD1. Refer to figure B-2 for the schematic diagram of the phase-shifter signal path. RF power divider PD1 splits the input RF signal four ways, with equal power distributed to each channel. No phase shift is introduced into the RF signals by the four-way power divider PD1. Consequently, one of the non-phase-shifted RF outputs at PD1 pin 4 is wired directly to the circuit board RF output connector J14.

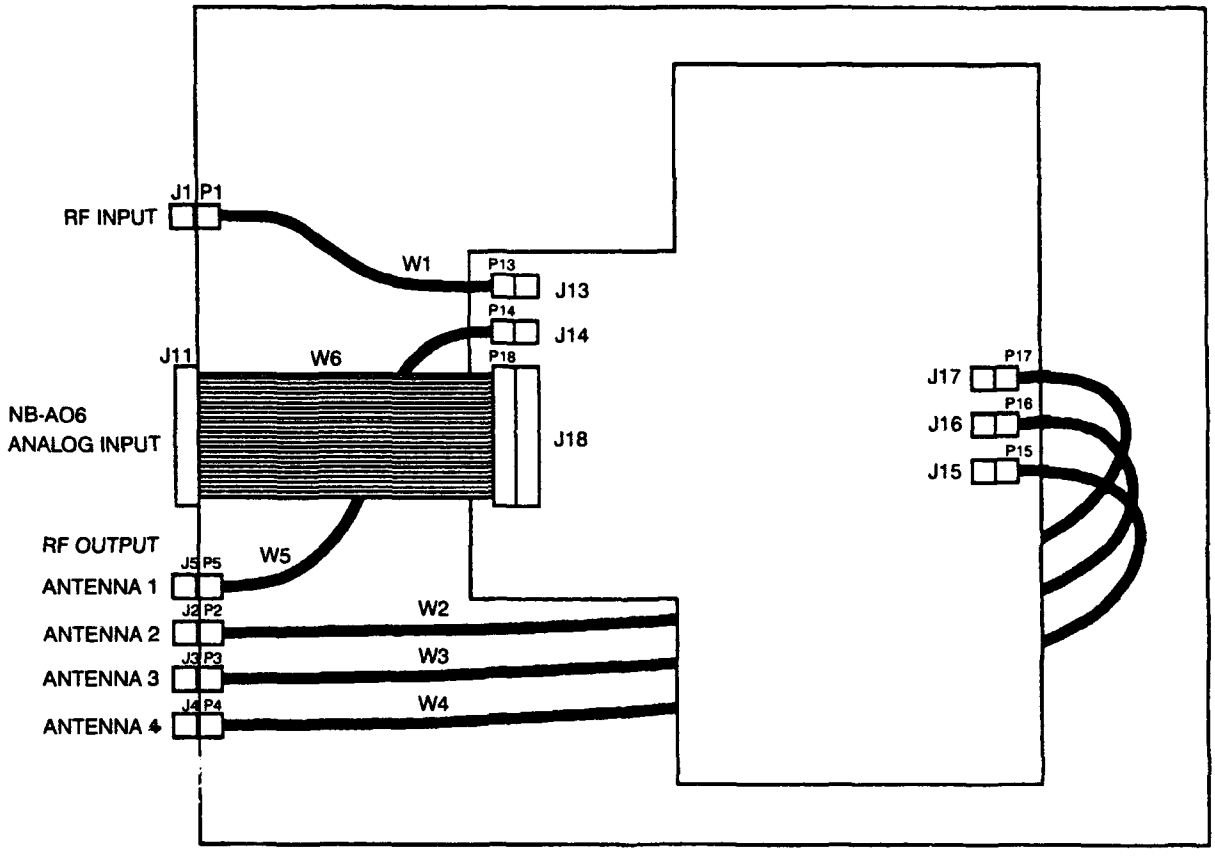

Figure 5. Simulator RF and analog interconnecting wiring diagram.

The circuit board RF output connector J14 is routed to Antenna 1 RF output connector J5 via RF cable W5. The Antenna 1 RF output is used as the baseline zero-phase-shift reference for the three remaining antenna outputs.

Alternately, the remaining RF output signals at power divider PD1 pins 1, 2, and 3 are routed to RF antenna outputs 2, 3, and 4 by the relay switching network of the selected-phase-shifter bank. The RF signal path for the 5-MHz relay switching network will be described in the

following paragraph. RF signal paths for the 12- and 25-MHz relay switching networks are similar to that of the 5-MHz network, although different relays and phase shifters are selected at these frequencies.

For 5 MHz, the RF output at power divider PD1 pin 1 is provided as an input to relay K2 pin 1. When the 5-MHz band is selected, relay K2 is enabled, closing the contacts between pins 1 and 7. The RF signal output at relay K2 pin 7 is provided as an input to the 5-MHz phase shifter, PS1 pin 1. The phase-shifted RF output at phase-shifter PS1 pin 3 is routed to the 5-MHz antenna enable relay, K15 pin 1. Since the 5-MHz band is selected, relay K15 is also enabled, closing the contacts between pins 1 and 7. The RF output signal at K15 pin 7 is wired directly to the circuit board RF output connector J17. Output connector J17 is connected to Antenna 2 RF output connector J2 via RF cable W2.

The two remaining RF antenna outputs use circuitry similar to antenna output 2. With 5-MHz selected, Antenna 3 uses power divider output PD1 pin 2, relays K6 and K15, phase-shifter PS2, circuit board RF output connector J16, RF cable W3, and Antenna RF output connector J3. Antenna 4 uses power divider output PD1 pin 3, relays K10 and K19, phase-shifter PS3, circuit board RF output connector J15, RF cable W4, and Antenna RF output connector J4.

If the RF bypass condition is selected, RF power divider output signals at PD1 pins 1, 2, and 3 are switched at relays K1, K5, and K9 directly to the output relays K16 and K20. While operating in this mode, the phase-shifter devices are bypassed, and no phase shift is introduced into any of the antenna RF outputs.

Antenna Phase Shift Control

Antenna phase-shift control signals originating from the NB-AO6 circuit board inside the Macintosh microcomputer enter the Simulator through rear panel connector J11 pins 4, 12, and 20. A 40-pin, mass-terminated ribbon cable, W6, connects the rear panel jack to the internal wire-wrap circuit board at connector J18, while maintaining the original input connector wiring pin outs. Refer to figure 5 for the RF and analog interconnecting wiring diagram. The input analog control signals at connector J18 pins 4, 12, and 20 are tied to the noninverting inputs (pin 11) of operational amplifiers (opamps) U3, U4, and U5 via voltage divider network U16. Refer to figure B-1 for the schematic diagram of the antenna phase-shift control circuitry. Voltage divider network U16 establishes a +14-VDC, mid-point, quiescent bias voltage at the opamp noninverting input terminal. A voltage regulator circuit sets the inverting input (pin 10) of opamps U3, U4, and U5 to this same +14-VDC level. Since the NB-AO6 unipolar output voltage swing is from 0 to +10 VDC (+5 VDC plus-or-minus 5 VDC), the output of the voltage divider network is +14 VDC, plus-or-minus 3 VDC. Consequently, this level-shifted signal centered at 14 VDC appears as a 6-VAC signal at the noninverting input terminal.

The gain of opamps U3, U4, and U5 is set by the 33 Ω feedback resistor (U3c, U4c, and U5c) and the input voltage divider network. The voltage gain is such that the 6-VAC input voltage swing will drive the opamp output through its entire +28-VDC range. The output of each

individual opamp (pin 6) is used to drive the selected voltage-variable phase-shift device. Figure B-2 shows the antenna-adjusted signal path through the relay switching network to the selected-phase-shifter bank.

+14-VDC Regulator Circuit

The +14-VDC regulator circuit consists of an LM317T adjustable 3-terminal positive voltage regulator and external biasing network U1 and U2. Refer to figure B-3 for the schematic diagram of the +14-volt regulator. Under normal operating conditions, the LM317T develops a nominal 1.25-VDC reference between the output terminal U2 pins 4/13 and the adjustment terminal U2 pins 3/14. This reference voltage is converted to a programming current by the 240-Ω resistor U2f, tied between the output and adjustment terminals. This constant current also flows through the fixed 1K-Ω resistor U2g, and the 2K-Ω trim pot U1a, thereby establishing the voltage regulator output with respect to ground. The current flowing from the adjustment terminal is held constant by the regulator circuitry and is limited to a 100-μA maximum. The contribution of the 100-μA adjustment current is negligible compared to the programming current flowing through the biasing network. As part of the biasing network, the 2K-Ω trim pot U1a allows for a precise adjustment of the output voltage and compensation for component aging.

+28-VDC Power Supply Voltage Monitor Circuit

The +28-VDC power supply voltage monitor circuit consists of operational amplifier U11, zener diode U8d, voltage divider network U8g and U8h, inverting Schmitt trigger U10, transistor array U12, series current limiting resistor network U9, and front panel LED display. Refer to figure B-1 for the schematic diagram of the +28-VDC power supply voltage monitor. Power supply voltage is monitored by using an LM1458 opamp (U11) as a high-gain voltage comparator operating open-loop without negative feedback. The voltage level at the inverting input of opamp U11 is fixed at approximately +20 VDC by the 1N968 zener diode U8d, and 12K-Ω current-limiting resistor U8e. Under normal operating conditions, the voltage divider network consisting of 27K-Ω resistor U8g, and 62K-Ω resistor U8h, establishes a voltage level at the noninverting input that is slightly higher than that of the inverting input, which is fixed by zener diode U8d. The more positive noninverting input drives the output of opamp U11 toward the top power supply rail of +28 VDC.

The +28-volt output at U11 pin 1 is connected to a voltage divider network consisting of 18K-Ω resistor U8b, and 82K-Ω resistor U8a. The voltage divider network reduces the +28-VDC output of opamp U11 to a TTL-compatible level of +5 volts maximum. The rapidly switched TTL-compatible level is subsequently shaped by two inverting Schmitt triggers U10 and used to forward-bias the +28-VDC display control transistor U12. The forward-biased transistor sinks current through the 150-Ω resistor U9f and drives the LED display, indicating that the +28-volt power supply is operating normally.

If, however, the +28-volt power supply output is reduced due to component failure or aging, the voltage divider output connected to the noninverting input at U11 pin 3 will fall below that

of the inverting input, which is held constant by zener diode U8d. At this point, the opamp output at U11 pin 1 will switch from approximately +28 VDC to nearly ground potential (zero volts). This low level output passed through the output voltage divider and Schmitt trigger inverters is not sufficient to forward-bias the +28-VDC display control transistor U12. For this reason, the front panel LED is extinguished, indicating a failure within the +28-volt power supply.

SIMULATOR SOFTWARE VIRTUAL INSTRUMENTS

PHASE TABLE CREATOR

The Phase Table Creator vi performs the characterization task for each of the voltage-controlled phase-shifter devices used within the Four-Channel HF Receiving Antenna Array Simulator. The characterization is tabulated in 5-degree increments throughout the entire 360-degree phase-shift range. At each 5-degree table entry point, the associated DC control voltage is recorded. The characterization table is stored in a file on the Macintosh computer's hard disk.

A single characterization table entry point is obtained by establishing a baseline DC control voltage at the phase-shifter adjustment terminals, sampling the receiver baseband audio outputs, using signal-processing techniques to estimate the relative phase shift between adjacent channels, and readjusting, if necessary, the control voltage in predetermined steps to obtain the desired phase angle within a specified resolution. In essence, this software control system initiates a trial and error process that adjusts the phase angle between adjacent receiver channels by incrementing or decrementing the phase-shifter DC control voltage based on the phase error measured at the receiver baseband audio output.

Since the characterization curve for the individual phase-shifter devices is, for the most part, nonlinear, successive 5-degree control voltage table entries are determined by applying a diminishing-step search algorithm. The algorithm advances the search for each table entry by incrementing the DC control voltage a specified amount from the previous setting. After an adequate settling time, the receiver baseband audio output is sampled and signal-processing techniques are used to make a relative phase estimate. If the amplitude of the control voltage is not sufficient to effect the desired phase shift, the voltage is increased by the previous step magnitude and a subsequent measurement is taken. If, however, the amplitude of the control voltage causes a phase-shift overshoot, the voltage is decremented by a step value one fifth the magnitude of the previous step. By diminishing the step size each time the desired phase angle is overshot, the hunting process quickly converges to the desired phase angle within the specified error resolution.

To adequately characterize the phase-shift circuitry throughout the HF band, phase tables are created at three discrete RF frequencies: namely 5 MHz, 12 MHz, and 25 MHz. At each frequency, a complete three-channel data file is created and stored on the Macintosh computer's

hard disk. These characterization data files are used extensively by the AAA Phase Tuner vi to adjust the antenna channel phase angles each time experiment data acquisition is initiated.

AAA PHASE TUNER VI

The AAA Phase Tuner vi is used to control the Four-Channel HF Receiving Antenna Array Simulator phase-shift circuitry during experiment data acquisition. To perform this task, the vi must first read the desired phase angle data from the experiment setup file, which is stored on the Macintosh computer's hard disk. The individual antenna channel phase angles stored in this file are derived from the signal direction of arrival input and the antenna spatial location input to the Select Experiment Parameters to Modify vi. Once the incident signal direction of arrival and the antenna array spatial locations have been established by experiment definition, the phase angles required to simulate these exact conditions for each antenna are calculated based on the known geometry of the given scenario. Once read from disk, these target phase angles are used to initiate a search for the DC control voltages required to tune the Simulator circuitry to these desired phase angles.

The empirical phase characterization data, which was tabulated by the Phase Table Creator vi, is used to calculate the DC control voltage required to drive the Simulator's phase-shifter circuitry. Since the phase angles will differ for each antenna channel, and may not intersect the tabulated 5-degree table entries, an interpolation between the nearest adjacent entry points must be performed to arrive at the initial DC control voltage settings. Also, the piecewise linear slope in volts per degree is calculated between these two nearest points for each antenna channel. The slope of the curve in the area of the desired phase angle can be used to fine-tune the adjustment process, should the initial setting yield a phase angle outside the specified resolution.

To begin the tuning process, the AAA Phase Tuner vi applies the DC control voltages that were derived from the interpolated table data to the Simulator phase-shift circuitry, allows for a brief settling period, then measures the resulting phase angles at the receiver baseband audio outputs. If additional fine tuning is required, the relative phase error (in degrees) measured at the receiver output is multiplied by the characterization curve piecewise linear slope (in volts per degree) to arrive at the next control voltage setting. This automatic process is repeated until the desired phase angles are achieved within the specified resolution on each antenna channel at the receiver baseband audio outputs.

CONCLUSIONS

Since its fabrication, the Simulator has been successfully used to test and evaluate adaptive array technology. As an integral part of the NRaD adaptive array test facility, the Simulator has become a valuable experimentation tool, capable of creating repeatable, complex electromagnetic scenarios with ease of operation by using a Macintosh computer and a graphical programming environment.

RECOMMENDATION

It is recommended that the Antenna Simulator be maintained to support the test and evaluation of future adaptive array algorithms.

Appendix A

DESCRIPTION OF GRAPHICAL PROGRAMMING LANGUAGE SOFTWARE

The Four-Channel HF Receiving Antenna Array Simulator is remotely controlled by a Macintosh microcomputer using National Instruments' LabVIEW graphical programming language software. The LabVIEW software, augmented by a suite of National Instruments NB-series NuBus I/O boards, is capable of simultaneously driving the Simulator phase-tuning circuitry, acquiring the HF receiver baseband audio outputs, performing signal processing, creating permanent files on magnetic media, and maintaining a graphical display on the Macintosh computer monitor.

The LabVIEW graphical programming environment is used to create what National Instruments has termed the Virtual Instrument or vi. The top layer of each vi consists of a graphically displayed control panel that is used to initiate program execution and to enter and display data. Each front-panel graphical display consists of user placed indicators and controls that resemble knobs, toggle switches, LED's, as well as scope and strip charts. Controls and indicators can be custom-labeled, scaled or sized, colored, and positioned anywhere within the bounds of the control panel drawing surface. In this way, unique vi's can be easily created for application-specific tasks that would otherwise require complicated integration of actual hardware components.

The underlying block diagram associated with the vi front panel appears on a second layer and graphically depicts the functional blocks of the task process. Each functional block appears as an icon on the diagram display, and is labeled, drawn, or shaped to help identify the functional process being performed. The various icons are interconnected by colored wires, which are used to indicate the data types of the parameters being passed from one function to the next. These data types can be integers, real numbers, booleans, arrays, and even clusters of several different data types, to name a few. The functional blocks can range in complexity from simple arithmetic calculations to sophisticated signal-processing techniques.

For more elaborate processes, common programming control structures can also be incorporated. These structures include For and While loops, Case statements, Sequence frames, and Formula nodes. Each control structure appears as yet another graphical window on the diagram, which contain user-defined functions to be performed once the structure is executed. Although LabVIEW can execute various portions of a process simultaneously, an execution order is usually defined by the user, especially when real-time I/O processes are being performed. For the most part, a data dependency will establish execution order, where all inputs to a function must be present before that portion of the process can be executed. Together, the combination of built-in LabVIEW functions with available control structures gives the user the

same flexibility of sophisticated high-level programming techniques without the syntactic debugging penalty associated with writing individual lines of code.

Another powerful LabVIEW attribute is the ability to nest entire vi's (called sub-vi's) within another higher level LabVIEW process (the calling vi). This is done by using the built-in LaBVIEW icon editor to create custom postage-stamp-sized icons for each subordinate vi process. The vi's front panel controls and indicators are assigned entry/exit points on the newly created icon, allowing the entire vi process to be nested within yet another higher level vi. Once an icon has been created using the icon editor, a suitable connection pattern is selected from the icon connector pane. There are 33 different patterns available that allow a range of one to twelve input or output nodes. Since multiple I/O data types can be clustered together on a single line, the maximum number of nodes an icon can support will not limit the ability to create I/O intensive vi's. The process of creating and nesting vi icons was used extensively while creating the Simulator control system vi's.

Appendix B

SIMULATOR SCHEMATICS

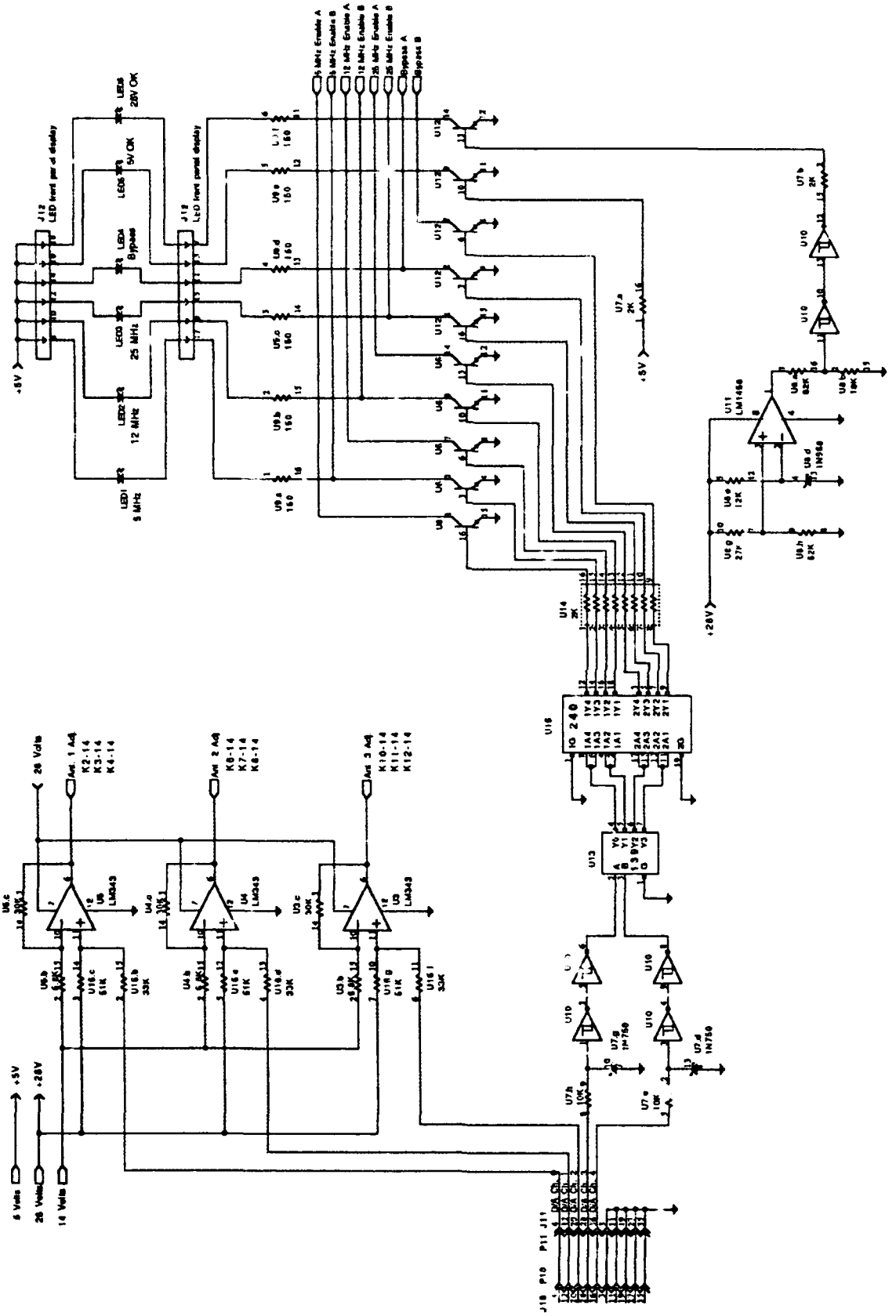

Figure B-1. Circuitry for relay and display control, phase-shift control, and power supply monitor.

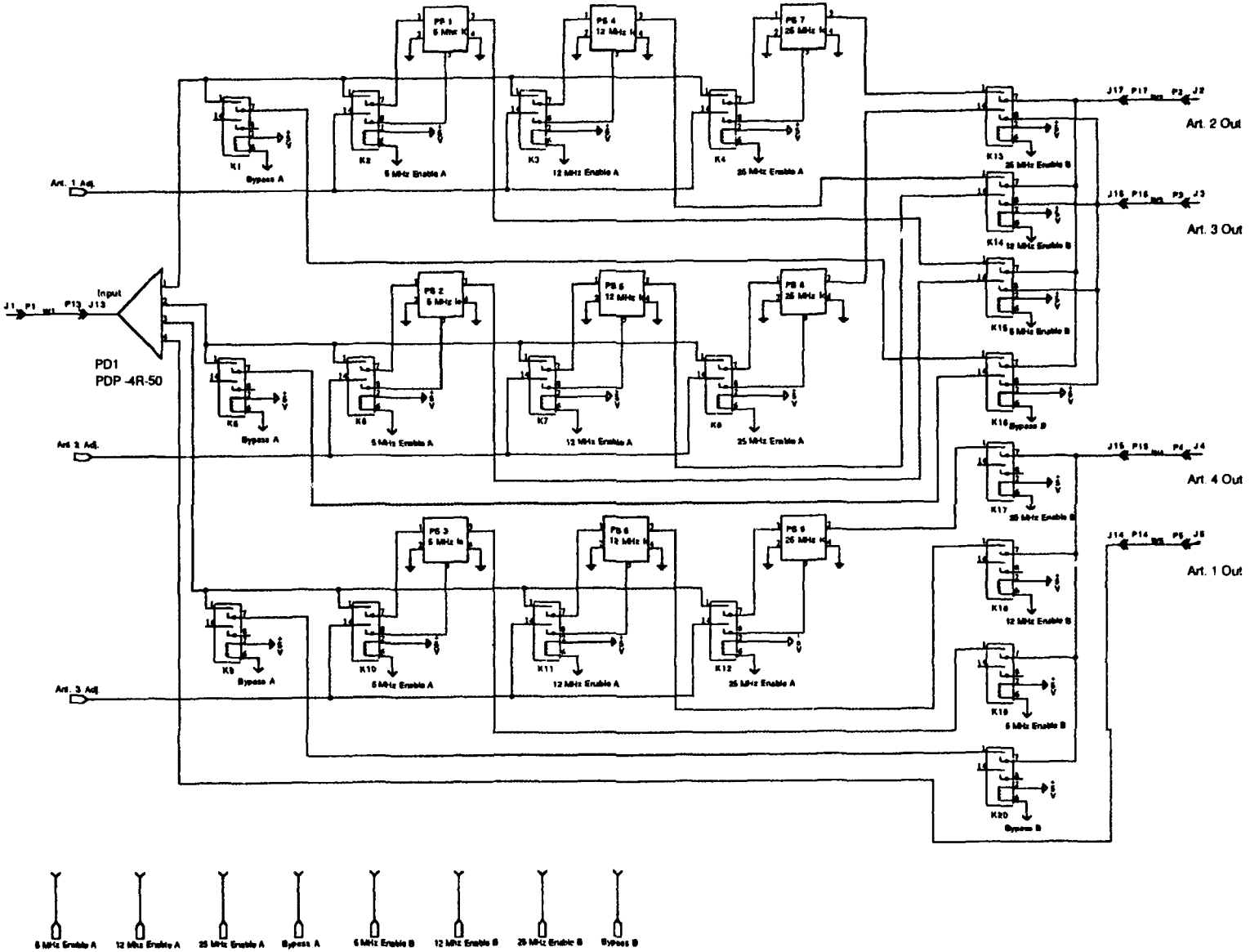

Figure B-2. Relay switching control and RF phase-shifter signal path schematic.

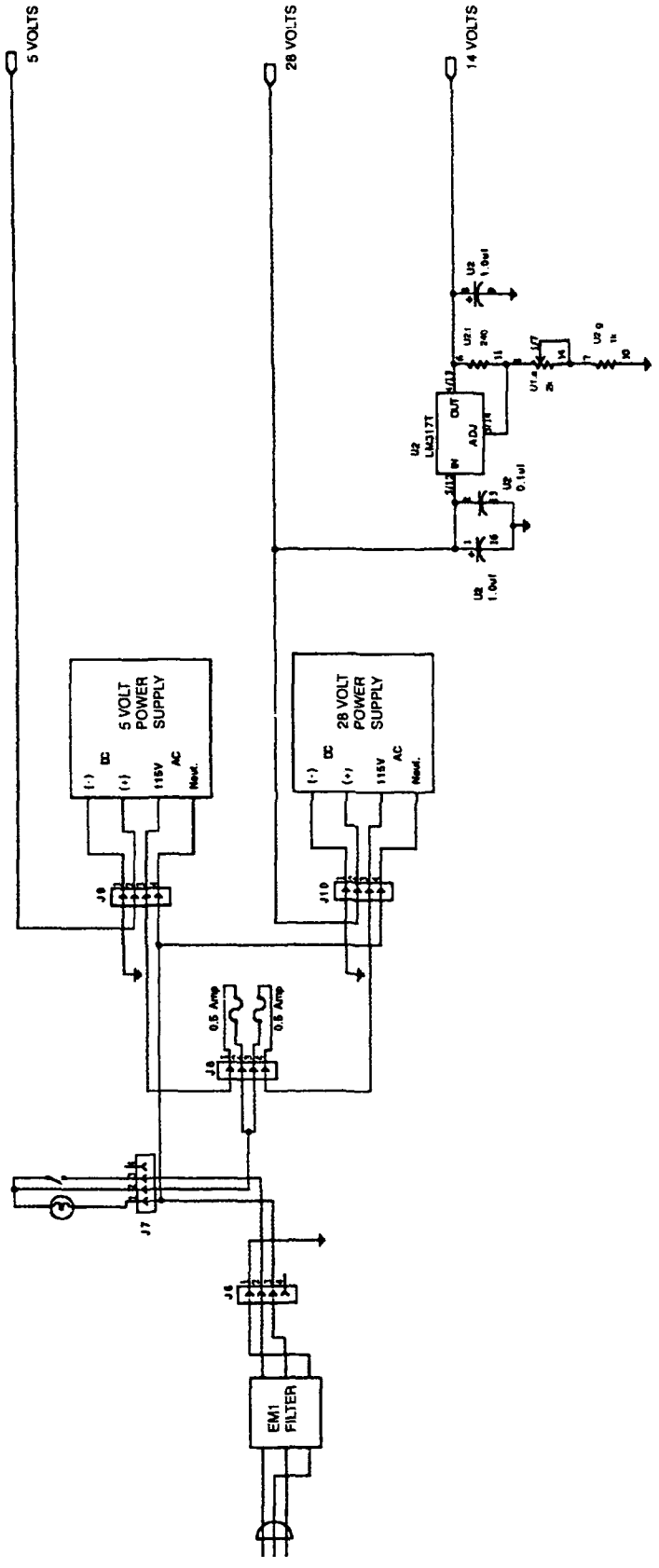

Figure B-3. 14-VDC regulator schematic.

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This document discusses the design, fabrication, and operation of an antenna array simulator, which is an integral part of the NRaD adaptive array evaluation facility. A brief introduction is provided to explain how adaptive receiving antenna arrays can improve Navy high-frequency communications, and how this developmental work is supported at NRaD. The main body of the text encompasses both the software algorithms created to support computerized remote control and antenna phase-tuning operation, as well as a detailed hardware description of the Simulator circuitry, which is suitable as a guide for maintenance and troubleshooting tasks.

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